

Methods and apparatus for implementing memory efficient LDPC decodes are described. In accordance with the invention message information is stored in a compressed state for check node processing operations. The state for a check node is fully updated and then subject to an extraction process to generate check node to variable node messages. The signs of messages received from variable nodes may be stored by the check node processor module of the invention for use in message extraction. The check node processor can process messages in variable node order thereby allowing the variable node processor and check node processor to operate on messages in the same order reducing or eliminating the need to buffer and/or reorder messages passed between check nodes and variable nodes. Graph structures which allow check node processing on one graph iteration to proceed before the previous graph iteration has been completed are also described.