

The present invention defines a family of logic circuitry comprising at least one logic gate. Each logic gate comprises a plurality of chalcogenide threshold switches (OTS1, OTS2, OTS3). The logic gates of the present invention use a chalcogenide threshold switch (OTS3) as a means of discharging load capacitance and resetting logic gate output. The present invention also defines a display driver for driving a flat panel display having row and column driving lines. The display driver comprises logic gates where each logic gate is comprised of chalcogenide threshold switches (OTS1, OTS2, OTS3).