

The invention relates to a circuit for generating negative voltages, comprising a first transistor (Tx2), the first terminal of which is connected to an input terminal (E) and the second terminal of which is connected to an output terminal (A) of the circuit, and the gate terminal of which is connected to a first clock pulse terminal via a first capacitor (Cb2). The circuit further comprises a second transistor (Ty2), the first terminal of which is connected to the gate terminal of the first transistor (Tx2), the second terminal of which is connected to the second terminal of the first transistor (Tx2), and the gate terminal of which is connected to the first terminal of the first transistor (Tx2). In addition, the circuit comprises a second capacitor (Cp2), the first terminal of which is connected to the second terminal of the first transistor (Tx2) and the second terminal of which is connected to a second clock pulse terminal. The transistors (Tx2, Ty2) are MOS transistors configured in a triple-well structure. The first terminal of a third transistor (Tz2) is connected to the second terminal of the first transistor (Tx2), the second terminal of said third transistor (Tz2) is connected to the trough(s) (Kw) housing the transistors (Tx2, Ty2, Tz2), and the gate terminal of the third transistor (Tz2) is connected to the first terminal of the first transistor (Tx2).

