

Additive Fibonacci generator with delay relates to information security systems, and other systems for simulation and modeling of random processes with high statistical characteristics. Additive Fibonacci generator includes combinational delay adder and  $q + 1$  memory registers, clock inputs are connected to the clock input device inputs information of each subsequent register memory connected to the output of the previous register memory outputs, the first register memory connected to the first input of the adder Raman, the second group of inputs is connected to the output register  $q$ -th memory and outputs Raman adder connected to the information inputs 0-th register memory. Further comprising logic circuit, information of which inputs connected to the outputs of the 0-th register memory device outputs, control inputs are connected to the control inputs of the device, and its output connected to the input adder transfer Raman. In the additive Fibonacci generator with a delay due to the introduction of new design elements and connections provided by increasing the initial period of repetition sequences of pseudorandom numbers and bits and improving their statistical characteristics, which greatly improves the characteristics of information security systems and other systems that use the proposed device.