

The device for express control of heart arrhythmia contains the generator of the timed pulses, the source of the constant potential, the set-point device for the constant potential with its input connected to the output of the source of the constant potential, the threshold element with its information input connected to the input of the device and the input of introducing the threshold of actuation connected to the output of the set-point device for the constant potential, the first pulse generator, the shift loop with its shift input connected to the output of the threshold element via the first pulse generator, the second and third pulse generators with their inputs connected to the third and fourth outputs of the shift loop, the first and second elements I with their first inputs connected to the output of pulse generator and their second inputs connected to the with the first and second outputs of the loop, respectively, the first and second delay elements with their inputs connected to the outputs of the second and third pulse generators respectively, the first and second pulse counters with their counting inputs connected to the outputs of the first and second elements I respectively and their reset inputs connected to the output of the second delay element, the first comparator connected digit-by-digit by its first and second inputs to the outputs of the first and second pulse counters respectively, the first and second groups of elements I with their first inputs connected digit-by-digit to the outputs of the first and second pulse counters respectively and their second inputs connected to the first output of the first comparator, the third and fourth groups of elements I with their first inputs connected digit-by-digit to the outputs of the first and second pulse counters respectively and their second inputs connected to the third output of the first comparator, the arithmetic unit with its control input connected to the output of the first delay element, the fifth group of elements I with its first inputs connected to the output of the third pulse generator and its second inputs connected digit-by-digit to the outputs of the arithmetic unit, the third unit I with its first input connected to the output of the third pulse generator and its second input connected to the second output of the first comparator, and the memory register with its reset input connected to the output of the second pulse generator, its first information inputs connected digit-by-digit to the outputs of the fifth group of the elements I, and its second information input connected to the output of the third element I.